Program: BE Electronics Engineering

Curriculum Scheme: Revised 2016

Examination: Third Year Semester VI

Course Code: EXC 603 and Course Name: VLSI DESIGN

Time: 1 hour Max. Marks: 50

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Note to the students: - All the Questions are compulsory and carry equal marks.

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| Q1. | In layout diagram which material is used for gate |
| Option A: | Polysilicon |
| Option B: | Si |
| Option C: | Ge |
| Option D: | GaAs |
|  |  |
| Q2. | In constant voltage scaling which parameter is constant |
| Option A: | voltage |
| Option B: | current |
| Option C: | power |
| Option D: | Voltage & current |
|  |  |
| Q3. | In voltage transfer characteristics of MOSFET inverter VIH indicates |
| Option A: | Cut off point |
| Option B: | Critical point |
| Option C: | Saturation point |
| Option D: | Depletion point |
|  |  |
| Q4. | Difference between Flip flop & latch is |
| Option A: | In flip flop clock is used |
| Option B: | In latch clock is used |
| Option C: | In flip flop & latch clock is used |
| Option D: | Clock is not used in flip flop & latch both |
|  |  |
| Q5. | In voltage transfer characteristics of MOSFET inverter VOH indicates |
| Option A: | Max output voltage when output level is logic 0 |
| Option B: | Minimum output voltage when output level is logic 0 |
| Option C: | Max output voltage when output level is logic 1 |
| Option D: | Minimum output voltage when output level is logic 1 |
|  |  |
| Q6. | What VTC indicates in CMOS inverter |
| Option A: | Voltage transfer characteristics |
| Option B: | Voltage transient characteristics |
| Option C: | Voltage time characteristics |
| Option D: | Voltage timeline characteristics |
|  |  |
| Q7. | ID=µCOX W/L(VGS-VTH)2 the MOSFET will work in |
| Option A: | Cut off region |
| Option B: | Active |
| Option C: | Saturation |
| Option D: | Depletion |
|  |  |
| Q8. | Correct symbol of CMOS |
| Option A: |  |
| Option B: |  |
| Option C: | CMOS - Wikipedia |
| Option D: | File:CMOS Inverter.svg - Wikimedia Commons |
|  |  |
| Q9. | RCA vs CLA |
| Option A: | delay of RCA is high |
| Option B: | Delay of CLA is high |
| Option C: | delay of both are same |
| Option D: | there is no delay in RCA |
|  |  |
| Q10. | D flip flop is also called as |
| Option A: | Delay flip flop |
| Option B: | dead flip flop |
| Option C: | deadline flip flop |
| Option D: | Double flip flop |
|  |  |
| Q11. | Channel length modulation parameter is |
| Option A: | λ |
| Option B: | Ω |
| Option C: | Δ |
| Option D: | β |
|  |  |
| Q12. | CCMOS stands for |
| Option A: | Complementary CMOS |
| Option B: | Clocked CMOS |
| Option C: | Control CMOS |
| Option D: | Complementary symmetry CMOS |
|  |  |
| Q13. | In Precharge & evaluate logic |
| Option A: | Common clock is given |
| Option B: | Different clock is given |
| Option C: | Clock is not given for Precharge logic |
| Option D: | Clock is given only for evaluate logic |
|  |  |
| Q14. | How many transistors are used in DRAM |
| Option A: | 5 |
| Option B: | 6 |
| Option C: | 4 |
| Option D: | 3 |
|  |  |
| Q15. | Which architecture is used to design VLSI |
| Option A: | System on device |
| Option B: | Single open circuit |
| Option C: | System on chip |
| Option D: | System on a circuit |
|  |  |
| Q16. | Which provides higher integration density? |
| Option A: | Switch transistor logic |
| Option B: | Transistor buffer logic |
| Option C: | Transistor transistor logic |
| Option D: | System on device |
|  |  |
| Q17. | Charge sharing problem occurs in |
| Option A: | Dynamic logic |
| Option B: | Pseudo logic |
| Option C: | Static |
| Option D: | CCMOS |
|  |  |
| Q18. | PROM stands for |
| Option A: | Programmable ROM |
| Option B: | Program ROM |
| Option C: | Primary ROM |
| Option D: | Programmable random access memory |
|  |  |
| Q19. | The component used for DRAM is |
| Option A: | Capacitor |
| Option B: | Resistor |
| Option C: | Inductor |
| Option D: | metal |
|  |  |
| Q20. | The expression for carry in half adder is |
| Option A: | AB |
| Option B: | A’B |
| Option C: | AB’ |
| Option D: | A’B’ |
|  |  |
| Q21. | In CMOS inverter |
| Option A: | 1 NMOS & 1 PMOS is used |
| Option B: | 2 NMOS used |
| Option C: | 2 PMOS used |
| Option D: | 4 NMOS used |
|  |  |
| Q22. | Difference between static & dynamic CMOS |
| Option A: | Both are same |
| Option B: | In static clock is used |
| Option C: | In dynamic logic clock is used |
| Option D: | Extra transistors are used in static RAM |
|  |  |
| Q23. | CMOS behaves like |
| Option A: | AND GATE |
| Option B: | OR |
| Option C: | NOT |
| Option D: | EXOR |
|  |  |
| Q24. | In realization of Y=A+B how many transistors are required? |
| Option A: | 6 |
| Option B: | 4 |
| Option C: | 5 |
| Option D: | 1 |
|  |  |
| Q25. | In realization of Y=A\*B how many transistors are required? |
| Option A: | 6 |
| Option B: | 4 |
| Option C: | 5 |
| Option D: | 1 |